A Multistandard HF/ UHF-RFID-Tag With Integrated Sensor Interface and Localization Capability

Thomas Ussmueller, Daniel Brenk, Jochen Essel, Juergen Heidrich, Georg Fischer, and Robert Weigel

Institute for Electronics Engineering, Friedrich-Alexander University of Erlangen-Nuremberg, Cauerstr. 9, 91058 Erlangen, Germany

***Abstract*—This paper presents a passive multistandard HF/ UHF-RFID-tag implemented in a 0.13um bulk CMOS process. The RFID-tag consists of a multi-standard HF/ UHF frontend for both frequency bands at 13.56 MHz and around 900 MHz. The tag is enhanced with additional functionality for sensing and localization. The integrated sensor interface consists of a multiplexer, a temperature sensor and an ultra-low power SAR analog-to-digital converter, which features a sampling rate of 100 kHz at a power consumption of less than 700 nW. Additionally the tag supports its localization through an FMCW-radar working at 2.45 GHz.**

***Index Terms*—RFID, ADC, FMCW-radar, HF, UHF**

I. Introduction

In the past years radio frequency identification (RFID) technology gained a lot of interest for ubiquitous wireless sensor networks. In this field a wide range of different application scenarios and thus a multitude of different sensor nodes exists. Active sensor nodes, i.e. sensor nodes with their own energy supply, e.g. with a battery, are mainly used for high performance and/ or high range use cases [1]. In contrast passive RFID-tags use the ambient energy for their power supply. Typically the energy-harvesting approach is based on the rectification of the received wireless power. Hence passive RFID-tags are well suited for low cost and maintenance-free operation.

The used frequency band of the passive RFID-tag mainly influences the available data rate and puts an upper limit for its operation range due to regulatory and physical constraints. HF-RFID-tags operate in the nearfield of the reader antenna and thus the operational distance is between several centimeters and one meter. In contrast to HF-RFID-systems UHF-RFID-tags transmit their data and energy by means of the electrical far field and thus they offer a higher read range upto 10m [2]. The use of passive multistandard RFID-transponders, which are working at both HF and at UHF frequencies allow a flexible and ubiquitous use in maintenance-free wireless networks. This multistandard ability guarantees a high acceptance rate in the market, because existing HF and UHF readers can be used.

In addition to the basic functionality of an RFID-tag, which is the transmission of an unique identifier, future RFID-systems could provide additional functionality. Two of the most interesting features are an integrated passive sensor interface and a locatable RFID-tag. The additional integration of sensors allows several enhancements on existing solutions. One application example would be an integrated temperature sensor for the monitoring of a cold chain. Other possible use cases include a monitoring device for the remote and maintenance-free acquisition of tire pressure values.

RFID-systems with an integrated localization capability can be used in different new application areas, for example tracking of persons and objects: In logistics the management of store-rooms could be automated because the position of a container affixed with a UHF transponder can be detected. For automotive applications several functions of a car could already be activated when the person is moving towards it.

All this functionality is available with active RFID-tags, which have a separate battery for their power supply. In contrast this work presents a completely passive solution covering the afore mentioned functionality. Therefore when operating in the UHF mode only a few μW are available as supply for all functional blocks, including the circuits for sensing and localization, and thus a highly efficient rectifier and low power circuit design technique have to be used for all components of the RFID-tag [3].

The following section of this paper describes the overall system architecture of the RFID-tag. The detailed discussion of the sub-components starts with the description of the analog front-end in section III, followed by the ultra-low power analog-to-digital converter (ADC) in section IV. After that the localization capability of the RFID-tag is discussed in section V. For both the sensor interface and the localization, custom commands according to the EPC protocol are necessary. They are described in section VI. In section VII the verification of the complete RFID-tag with all its functionality is presented.

II. System Architecture

A typical state of the art passive RFID-system consists of an interrogator/reader and several passive transponders. The interrogator communicates with the transponders by a wireless peer-to-peer connection and is responsible for the power supply of the passive transponders.

978-1-4673-0328-6/12/$31.00 ©2012 IEEE

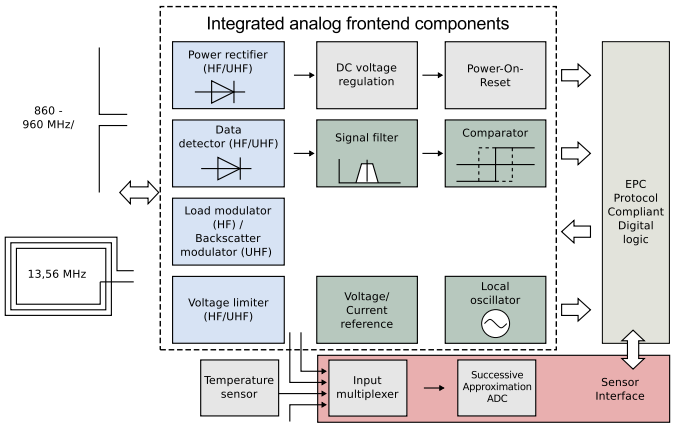


Fig. 1. System architecture of the passive Multistandard RFID-Tag with sensor interface and the switched passive reflector

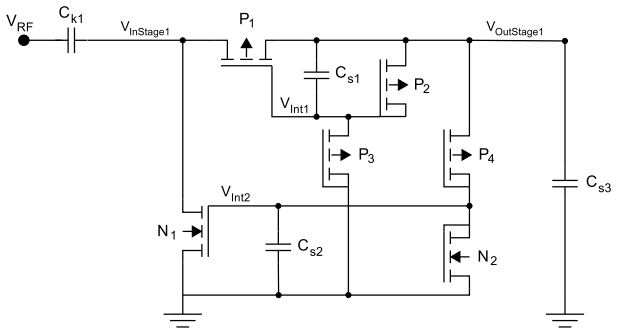


Fig. 2. First stage of the implemented rectifier with threshold cancelation circuit for UHF

Fig. 1 shows the block diagram of the implemented multi-standard RFID transponder. The only external component of this multistandard tag is the antenna which can be used at UHF and HF. This test chip has been integrated in a 0.13 µm digital CMOS technology.

The two combined highly efficient power rectifiers convert the incoming electromagnetic RF wave to DC in order to supply all active circuits on the transponder. If the DC supply voltage reaches a defined level, the power-on-reset generates a reset signal which places the digital part into a known state. The demodulator recovers the information, which is ASK modulated on the carrier by the interrogator and delivers the data to the digital part. The backscatter modulator at UHF and the load modulator at HF enable the tag-to-reader communication by varying the impedance of the RF node in order to modulate the reflected power (UHF) or by changing the load of the inductively coupled transformer network. The integrated voltage limiter protects the tag circuits at high RF levels. Different current sources have been designed to drive the various filters and references. In addition to the classical tag functionality an ultra-low-power sensor interface has been implemented as well. It consists of a four-to-one multiplexer, an integrated temperature sensor and a SAR analog-to-digital converter. The multiplexer connects either the internal temperature sensor, the received signal strength indicators of the UHF or of the HF frontend or an external analog sensor to the ADC.

III. Multistandard Analog Front-End

In this section, the most important analog building blocks of the RF frontend are presented. Because in analog RF frontends non-linear and time-variant components are coupled in a single node it is essential to know the behavior of the devices and the used technology for an ultra low-power frontend design.

A. Ultra-Low-Power Rectifier

To achieve a higher conversion efficiency without the use of Schottky diodes, the simple 2-stage voltage multiplier has to be modified. Fig. 2 shows the first stage (input stage) of the implemented rectifier with a threshold cancelation circuit for the rectifying transistor pair P_1 and N_1. The cancelation of the threshold voltage of the PMOS transistor P_1 is obtained by the two PMOS transistors P_2 and P_3 and the capacitance C_{s1}. The cancelation of the threshold voltage of the NMOS transistor N_1 is obtained by P_4, N_2 and C_{s2}. The two transistors P_3 and P_4 are used in their sub-threshold operating region as active high impedance resistors. The value of the resistance can also be affected by the bulk connection of the transistors. Using transistors as high impedance resistors saves chip area and thereby costs, as integrated resistors with a comparable value are very large. The simulated signal levels for the input voltage $V_{InStage1}$, the output voltage $V_{OutStage1}$ and the internal signals V_{Int1} and V_{Int2} are plotted in Fig. 3. These simulated signals are plotted for two periods of a 900 MHz input signal at an input power level of about -15 dBm. It is shown, that the signal V_{Int1} is reduced about the threshold value of the transistor P_1 in comparison to $V_{OutStage1}$. The signal V_{Int2} is increased by the threshold voltage of N_1. This threshold cancelation technique needs no additional reference voltages or currents to adjust these internal voltages. Therefore this self cancelation technique is already working at very low input power levels even if the DC voltage at the output of the rectifier is too low to supply auxiliary circuits.

Fig. 4 shows the complete 2-stage rectifier which is implemented in a 0.13 µm CMOS technology. Analogous to the first stage of the rectifier, the threshold voltage of the transistor P_5 is compensated by P_6, P_7 and C_{s5} and the threshold voltage of the transistor N_3 by P_8, N_4 and C_{s4}.

B. Tag-to-Reader Communication

Backscattering of the incident RF power is the communication principle used in passive UHF RFID-systems. The tag-to-reader communication is implemented by varying the impedance of the RF node's analog frontend in order to modulate the reflected power. There are two types of modulation allowed by the EPC UHF Class1 Gen2 standard for RFID backscattering communication: amplitude shift keying (ASK) and phase shift keying (PSK) [4]. Both modulate the complex impedance $\underline{Z}_m = R_m + jX_m$ (m = 1,2) between two different states. An ideal ASK modulation can only be achieved by a switching resistance if the imaginary part of

$\underline{Z}_m$ is zero. Otherwise a more complex modulation circuit is needed. It is demonstrated in [2] and [5] that the PSK modulation would be more efficient than ASK because the available power to the tag is kept almost constant during both modulation states. Analogous to the ideal ASK modulation a PSK modulation can be achieved by a complex modulation circuit only. Due to the fact, that most RFID-transponders are using a switched resistance or a switched capacitance and that several parasitic effects get more important at high frequencies, common integrated backscatter modulators use a combination of PSK and ASK. Therefore, the most reasonable modulation type depends on the available solid-state device technology.

In passive HF RFID-systems an integrated load modulator is used for the tag-to-reader communication. For this type of communication the transponder antenna has to be in the reactive near field of the reader antenna. Because of the transformational coupling between the coil of the transponder and the coil of the reader, a change of the transponder impedance can be detected by the reader. This change can be realized by a carefully designed MOS transistor between the input pins L_{A_HF} and L_{B_HF} which is driven by the digital baseband signal.

C. Reader-to-Tag Communication

The ASK demodulator is an important circuit block for the bi-directional data transmission between the RFID-transponder and the reader. It recovers the information, which is ASK modulated on the carrier by the interrogator and delivers the data to the digital logic. To achieve a higher reading range, the reception of data has to be ensured at low power levels. Because of different modulation depths and different input power levels for UHF and HF two demodulation blocks are used. Fig. 5 shows the simplified block diagram of the ASK demodulator for the UHF mode. The input signal $Env_{In,UHF}$ of the demodulator is the envelope of the carrier. This signal is initially level shifted by the non-linear resistors and then filtered by either the current source I_1 (upper path) or the current source I_2 and the capacitor C_1 (lower path). To receive the digital baseband signal, these two values with

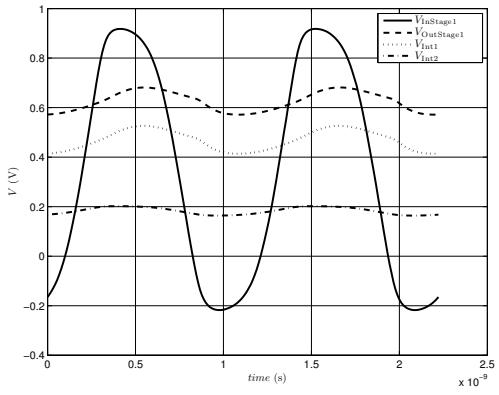


Fig. 3. Internal signals of the first rectifier stage

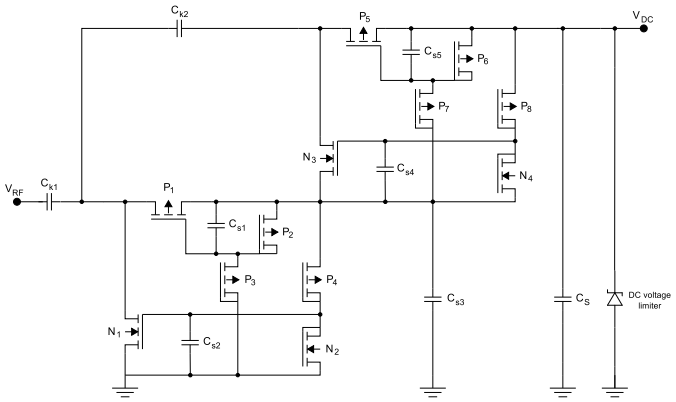


Fig. 4. Single-ended two-stage rectifier with threshold cancelation circuit for UHF

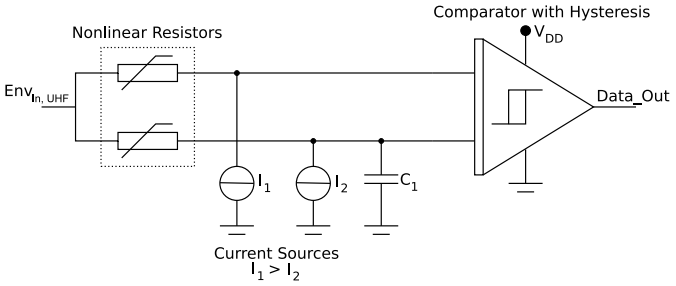


Fig. 5. ASK data detector (UHF)

different time constants and slightly different voltage levels are compared by a low-power comparator with hysteresis. The different voltage levels result from the different dimensions of the current sources I_1 and I_2 and assure a robust demodulation. Because these signals are generated from the same input signal the filters of both paths can be designed with a very low power consumption.

Fig. 6 shows the simplified schematic of the implemented HF demodulator. It looks very similar to the demodulator which is used for UHF. Due to the lower modulation depth in HF (HF: 10 - 30 % ASK, UHF: 80 - 100 % ASK) the used filter structures have to be designed more complex. To demodulate the very small change in the carrier's amplitude, the current sources have the same dimension to prevent different voltage levels. Only the time constant of the signals are adjusted by the capacitors C_1, C_2 and the resistor R_1. To assure a robust demodulation in HF the hysteresis behavior of the comparator

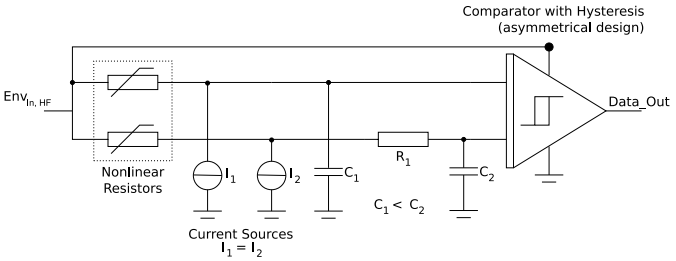


Fig. 6. ASK data detector (HF)

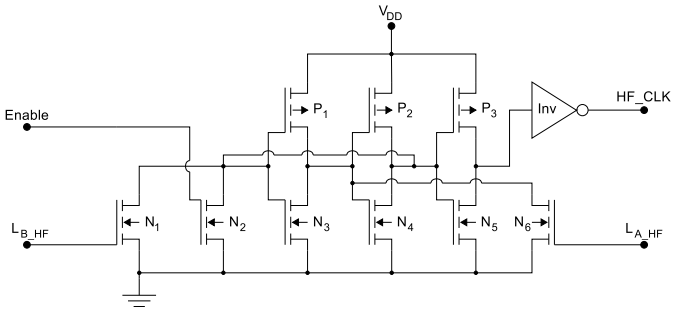


Fig. 7. Integrated circuit which recovers the 13.56 MHz clock from the differential input signal

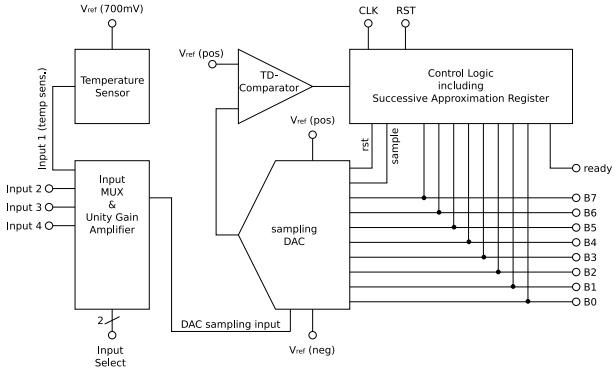


Fig. 8. Block diagram of the sensor interface including an input multiplexer, a temperature sensor, and an eight Bit successive approximation ADC with DAC-integrated sampling, and a time-domain comparator.

is amplified by an unsymmetrical design and the use of the modulation state dependent signal $Env_{In,HF}$ as supply voltage.

D. Clock Generation and Clock Recovery

In the UHF range the RF frequency is between 860 MHz and 960 MHz. Here, clock recovery is not suitable because the related power consumption would be too high. Therefore UHF transponders have to implement an own tag oscillator. Like the other transponder components, its architecture must meet low-voltage (typically 1.0 V to 1.5 V) and low-current ($\approx$ 1.5 µA) requirements. The related frequency value is influenced by different system parameters like temperature, supply voltage, phase noise or process variations. According to the EPC protocol for the UHF range frequency variations of the clock signal must be within a $\pm$ 4 % interval during the steady state ($\pm$ 2.5 % during the short period of backscattering). However, these requirements are well below the demands of modern communication systems, so simple components like RC oscillators can also be used [6]. The implemented clock generator is a relaxation-type oscillator working at 2.4 MHz.

Due to the lower carrier frequency a clock recovery circuit has to be used at HF. Fig. 7 shows the integrated circuit which recovers the 13.56 MHz clock from the differential input signal. Afterwards, the output signal *HF_CLK* is divided by the factor 8 for the use as the system clock of the transponder. The input pins L_{A_HF} and L_{B_HF} are connected to the corresponding HF input pins of the tag. The clock recovery circuit can be enabled by the *Enable* pin. The signal *Enable* is connected to $Short\_L_{B,HF}$ which defines the ground potential and switches off the clock recovery at UHF. At HF this signal is low and the recovery circuit is switched on. During the positive half-wave on $L_{A,HF}$, the transistor N_6 is switched on and the output *HF_CLK* is high, during the negative half-wave N_6 is switched off and N_1 is switched on and therefore the output is low.

IV. Sensor Interface

In Fig. 8 the architecture of the sensor interface is illustrated. On the left the ultra low current temperature sensor is shown, which is connected to the first of four multiplexer inputs. The sensor is implemented using the temperature effects on a diode-connected NMOS transistor which is supplied with a constant current. This current in turn is generated using

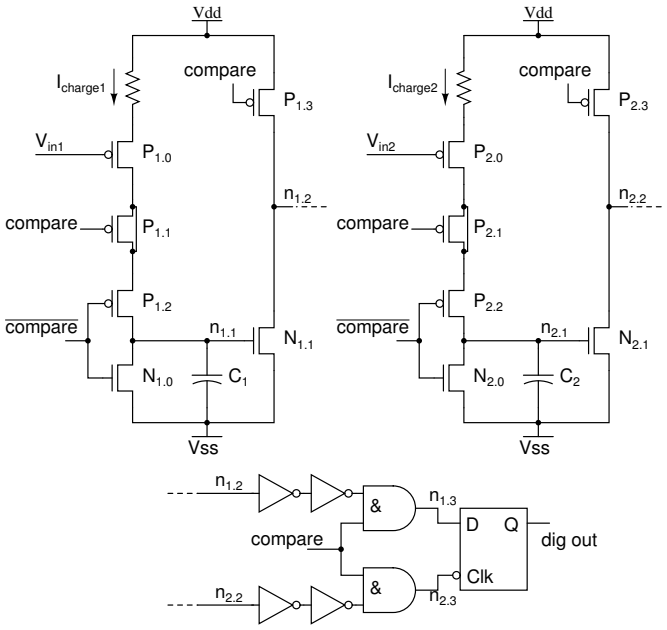


Fig. 9. Schematic of the time domain comparator.

the ZTC bias point technique mentioned in [7]. The unity gain buffer integrated into the multiplexer feeds the capacitive sampling DAC array of the ADC. The DAC is controlled by the ADC's logic and its analog output is linked to the time-domain comparator which represents the digitizing element of the sensor interface. As shown in [8], the time-domain technique keeps the current demand low for the comparator. The control logic is built using standard cells of the 0.13 µm CMOS process.

A. Time-Domain-Comparator

A comparator is needed to evaluate the DAC output signal in relation to the reference voltage and digitize each one-Bit result before it is stored in the approximation register. The designed time domain comparator circuit (TDC) is shown in Fig. 9. The input voltage signals V_{in1} and V_{in2} are converted to time domain signals by two identical and symmetrically

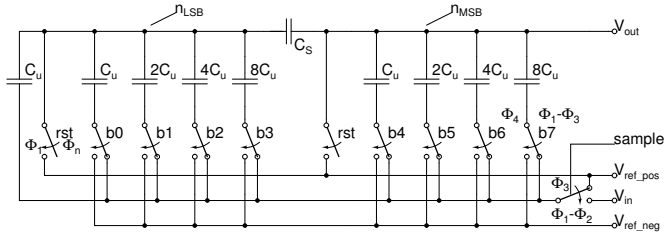
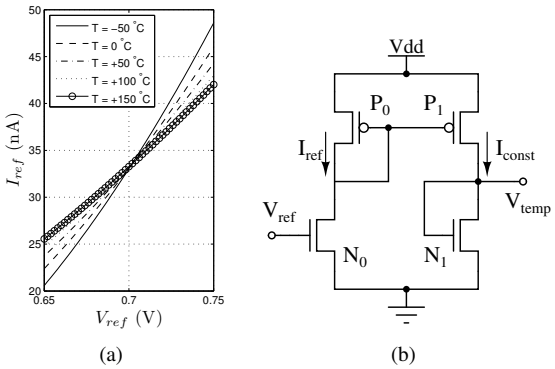


Fig. 10. Capacitive sampling DAC using charge scaling



(a) (b)

Fig. 11. Temperature sensor: (a) Illustration of the ZTC bias point of transistor N_0. (b) Schematic of the temperature sensor.

layouted circuit parts. This was already discussed in [8] and first mentioned by [9]. It was shown, that the speed limit for the compare-signal of the circuit is given by

$$f_{compare} < \frac{I_{charge}}{2CV_{t,n}} \tag{1}$$

with I_{charge} and C as depicted in Fig. 9 and $V_{t,n}$ as threshold voltage of NMOS transistor $N_{1.1}$ and $N_{2.1}$, respectively. A further optimization is reached by adding the dummy transistors $P_{1.1}$ and $P_{2.1}$ to minimize the clock feedthrough of the compare signal. This ensures a sensitivity of better than 1 mV which is sufficient for an LSB value of 1.96 mV.

B. Digital-to-Analog Converter

The SAR ADC uses for digital-to-analog conversion a capacitive DAC (CDAC). Charge redistribution [10] and charge scaling techniques were applied in this design. During one data conversion cycle the 8-Bit DAC shown in Fig. 10 performs the following steps: In phase Φ_1 the rst- and sample-switches are closed and b0...b7 are turned to the V_{in}-path. This way, the nodes n_{LSB} and n_{MSB} are initialized to the potential V_{ref_pos} and all lower capacitance plates to V_{in}. In phase Φ_2 the rst-switches are opened, conserving a charge proportional to $(V_{ref\_pos} - V_{in})$ on the upper plates. If the sample-switch is set to V_{ref_pos} in phase Φ_3, the potential at node n_{MSB} gets $(2V_{ref\_pos} - V_{in})$. When switching sequentially b7...b0 between V_{ref_pos} and V_{ref_neg} in phase Φ_4 (with V_{ref_neg} being V_{SS}), the output voltage V_{out} is described by the expression

$$\begin{aligned} V_{out} =& 2V_{ref\_pos} - V_{in} \\ & - V_{ref\_pos}\left(\frac{1}{16}\frac{\sum_{i=0}^{3} b_i 2^i + 1}{2^4} + \frac{\sum_{i=0}^{3} b_{4+i} 2^i}{2^4}\right). \end{aligned} \tag{2}$$

The previously conserved charge on the top plates corresponding to $(2V_{ref\_pos} - V_{in})$ represents the sample offset. Thus the CDAC is also used as sample and hold circuit. The minimum S&H capacity for an ADC is determined by the voltage step corresponding to the LSB. This unipolar 8-Bit ADC works with a reference voltage of 500 mV and has an LSB voltage of 1.96 mV. The sampling noise voltage of an unipolar ADC is given by

$$v_{n,sample} = \sqrt{\frac{kT}{C_{sample}}}. \tag{3}$$

The complete DAC capacitance (depicted in Fig. 10) is 31 C_u which equates to C_{sample}. As the unity capacitance C_u is 59.3 fF including all parasitic components, the resulting sampling noise voltage is 48 µV, which is well below the LSB value of 1.96 mV. This demonstrates, that the sampling noise for CDACs only has to be considered for ADC designs above 10 Bit resolution. The reason for the unity capacitance being much bigger than needed with respect to the sampling noise is the matching requirement between the single unity capacitances among each other and related to the scaling capacitance. It is shown in [11] and [12], that the scaling capacitance in a capacitive charge scaling DAC should be dimensioned according to

$$C_S = C_u \frac{2^{N/2}}{2^{N/2}-1} = \frac{sum(C_u, LSB)}{sum(C_u, MSB)} \tag{4}$$

were N is the resolution of the DAC. The sum of all unity capacitances in the LSB-array is the numerator and the sum of all unity capacitances in the MSB-array is the denominator. A dual 4-Bit charge-scaling CDAC would need a C_S value of 16/15 C_u.

C. Temperature Sensor

The integrated temperature sensor is based on the existence of a zero temperature coefficient (ZTC) bias point of MOS transistors as described by Filanovsky and Lim in [13] and later shown by Zhai et al. in [14]. At this bias point the temperature effects on electron mobility μ and threshold voltage V_T compensate each other. This results in a constant drain current I_D over temperature as illustrated in Fig. 11(a). The circuit shown in Fig. 11(b) requires a reference voltage V_{ref} to generate a reference current I_{ref} through N_0. By using a current mirror (P_0, P_1), an equivalent constant current I_{const} is generated. As the current is stable over temperature, the voltage drop V_{GS} over N_1 is given by [13]

$$V_{temp} = V_{GS} = V_{GSF} + \alpha_{VT} T \left(1 - \sqrt{\frac{I_D}{I_{DF}}}\right) \tag{5}$$

where V_{GSF} and $I_{DF} (= I_{const})$ are the parameters of the common intercept point of both temperature dependent characteristics (μ & V_T) and α_{VT} is the threshold voltage temperature coefficient. V_{temp} is a linear function of the temperature T.

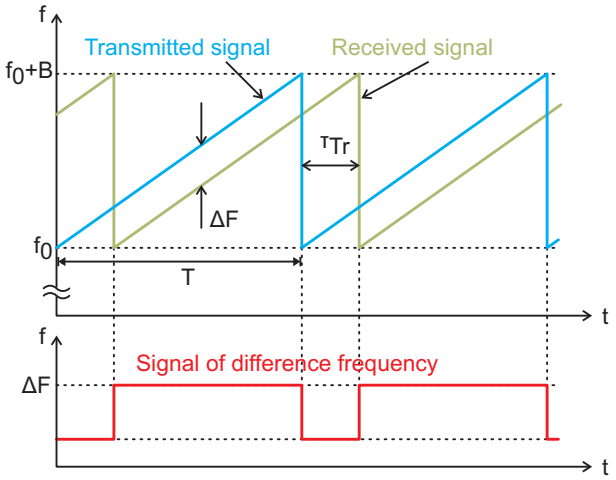


Fig. 12. Frequency curve of transmitted and received FMCW signal

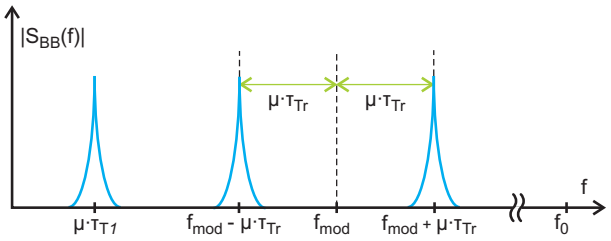


Fig. 13. Baseband spectrum with modulation

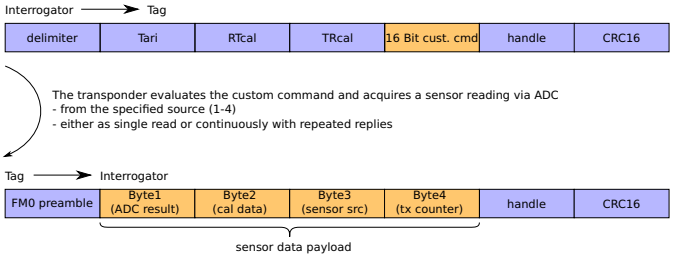


Fig. 14. A sensor data acquisition is triggered with a standard compliant custom command. The result is transmitted in a compatible encoding but with a non-standard frame structure.

As the current through a MOS FET mainly depends on the gate source voltage, the solution shown in [14] would need an additional voltage stabilizing circuit for V_{dd} (e.g. a low dropout regulator). Within a passively supplied RFID the supply voltage V_{dd} is highly fluctuating. This is the reason for generating the temperature independent current with a NMOS transistor instead of using the ZTC bias point of a PMOS transistor.

V. Distance Measurement

The localization principle of the RFID-tag is based on a FMCW radar system with modulated reflection. The FMCW reader transmits a continuous wave signal with a linear frequency modulation. The signal starts at a lower frequency f_0 and is within the modulation interval linearly increased in frequency to an upper frequency of $f_0 + B$ (Fig. 12).

The signal from the FMCW reader is reflected at the antenna of the RFID-transponder at the distance d and at any other target close to the reader, too. Therefore the reflection coefficient of the transponder antenna is characteristically modulated after activating the distance measurement with the related custom command. Thereby it can be distinguished from false targets in the operating range of the reader.

The modulation frequency of about 300 kHz is derived from the internal clock generator of the RFID-tag by a divide-by-8 frequency divider. This modulation should be performed for the duration of a modulation interval T of the FMCW reader to use its whole bandwidth B. This is important for a good resolution of the distance measurement [15]. The backscattered signal of the transponder arrives at the antenna of the reader delayed by the run-time τ_{Tr}. This signal is then mixed with the transmitted signal [16].

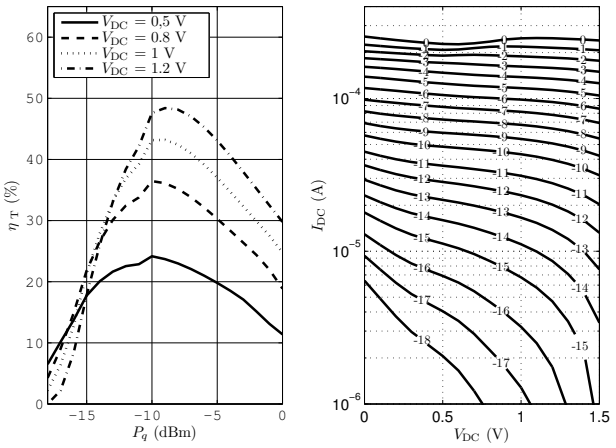
The signal at the output of the mixer for the duration of one ramp interval T is then digitized and the further data processing is done in the digital domain. The related baseband spectrum is not dependent on time. It consists of two mainlobes around a center frequency f_{mod} (Fig. 13). Its value is given by the modulation frequency f_{mod} of the transponder. The distance Δf of the two mainlobes depends on the distance d between reader and transponder and the known ramp frequency. In [15] a detailed insight into radar theory is given.

VI. Communication Protocol

The data conversion as well as the localization is triggered by using custom commands declared in the RFID protocol standard *EPC UHF class1 gen2* [4]. The range from 0xE000 to 0xE0FF is reserved for these commands, resulting in 256 possibilities to trigger own actions not described by the standard. Tab. I shows the custom commands used for sensor data acquisition within the UHF RFID test system. These custom commands were added to the finite-state machine of the transponder already containing all mandatory EPC commands. If a single sensor reading shall be taken from source 3, the corresponding custom command that is sent to the RFID Transponder is 0xE0E8. After the command code is sent within an established EPC session, the ADC starts a conversion on the specified input source and the acquired sensor data is transmitted back to the UHF RFID reader as shown in Fig. 14. The actual sensor reply consists of four Bytes: ADC data, ADC calibration data, sensor source information and a counter. The ADC calibration data Byte is

TABLE I
Custom Command-DEFINES FOR THE SENSOR EXTENSION FUNCTIONALITY.

Code	Parameter 1 (Source)	Parameter 2 (Function)
0xE0EX	X = 0b00xx → src 1	X = 0bxx00 → single
	X = 0b01xx → src 2	X = 0bxx01 → continuous
	X = 0b10xx → src 3	X = 0bxx10 → reserved
	X = 0b11xx → src 4	X = 0bxx11 → reserved



(a) (b)

Fig. 15. Efficiency (a) and IV-characteristic (b) of the integrated UHF rectifier

reserved for future use and was set to a constant (0x55) at the current state. The sensor information links the ADC data received by the reader to a specific sensor source. Depending on the command mode (single or continuous), the acquisition and data transmission takes places only once or infinitely until the supplying field is switched off. Using the latter mode requires no further interaction from the reader device. In this mode the counter increases with each conversion, providing a timestamp-like identification of the ADC data. All 256 acquisitions the counter gets an overflow and starts at 0x00 again.

VII. Experimental Results

A. Ultra-Low-Power Rectifier

Fig. 15(a) shows the measured efficiency and Fig. 15(b) the measured IV-characteristic of the proposed rectifier circuit at UHF. For a DC output power of 10 uW (1 V and 10 uA) the efficiency is about 25 %. The maximum efficiency for a DC output voltage of 1 V is about 43 % and the efficiency of the rectifier at -15 dBm RF input power is still 20 %.

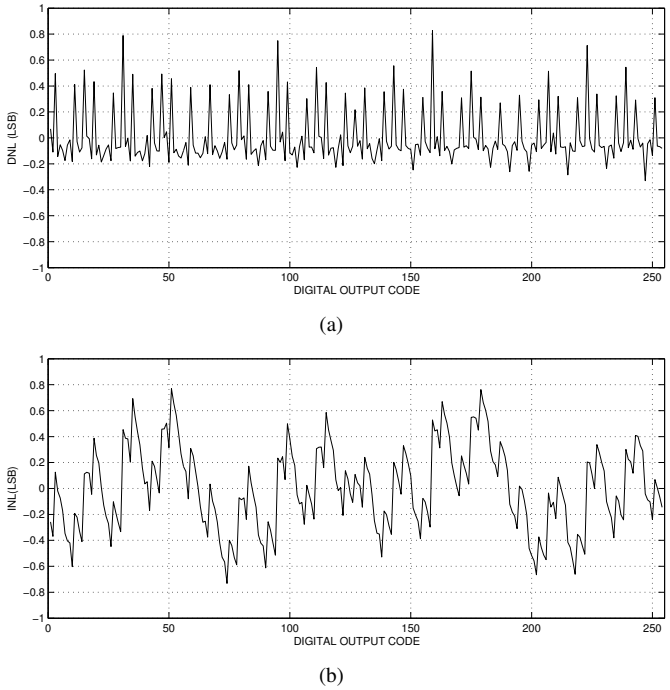
These measurements are done with a computer controlled automatic multi-purpose source tuner. This tuner uses three independent wide-band probes to control the amplitude and phase of the reflection factor. With this tuner it is possible to use two probes for pre-matching to achieve a very high VSWR. This is absolutely essential because otherwise it is not possible to characterize the behavior of the rectifier or to perform efficiency measurements. To facilitate the handling, the analog frontend has been soldered on a custom made test fixture.

B. ADC Characterization

The SAR ADC test chip was characterized statically and dynamically. The differential (DNL) and integral non-linearity (INL) were acquired using the histogram method at a very low input frequency (f_{in} = 22 Hz). Fig. 16(a) plots the DNL over the digital output code. The values are between -0.36 and +0.81 LSB. In Fig. 16(b) the corresponding INL is plotted with values between -0.75 and +0.75 LSB. Dynamic tests resulted in a stable performance for different input- and sample-frequencies. Signal-to-Noise-and-Distortion ratios (SNDR) of 46 and 41.9 dB are reached at a sample rate of 40 kSps for low- and nyquist-frequency input signals, resulting in an effective resolution of 7.36 and 6.68 Bit, respectively. In both cases, the current is less than 700 nA. When lowering the supply voltage, the power demand diminishes but the harmonic distortions increase. At 0.9 V (leaving all other operating conditions as is) the current consumption drops to 525 nA and a still acceptable effective number of bits (ENOB) of 7.23 is reached. It has to be stated, that the source meters used for the supply- and reference voltage added a not negligible noise voltage to V_{DD} and V_{ref_pos} that could not completely be eliminated by low-pass buffer capacitances. When using a better, less noisy reference voltage, better effective resolutions than 7.36 Bit can be reached. The ADC consumes depending on temperature and sample rate 525 nA to 1.65 µA. Especially measurements at supply voltages above 1 V and at higher temperatures ($> 80\,^{\circ}$C) show high leakage conditions.

C. RFID System Tests

UHF range measurements with the commercial UHF-RFID-reader at 2 W transmit power and the sensor-transponder showed operational distances of up to 8 m. Additional sensor measurements using our custom command-capable UHF reader at the lower transmit power level resulted in similar distances for sensor- and non-sensor operation. This indicates that the ADC - which is turned off for non-sensor operation -



(a)

(b)

Fig. 16. DNL (a) and INL (b) of the ADC acquired with the histogram method.

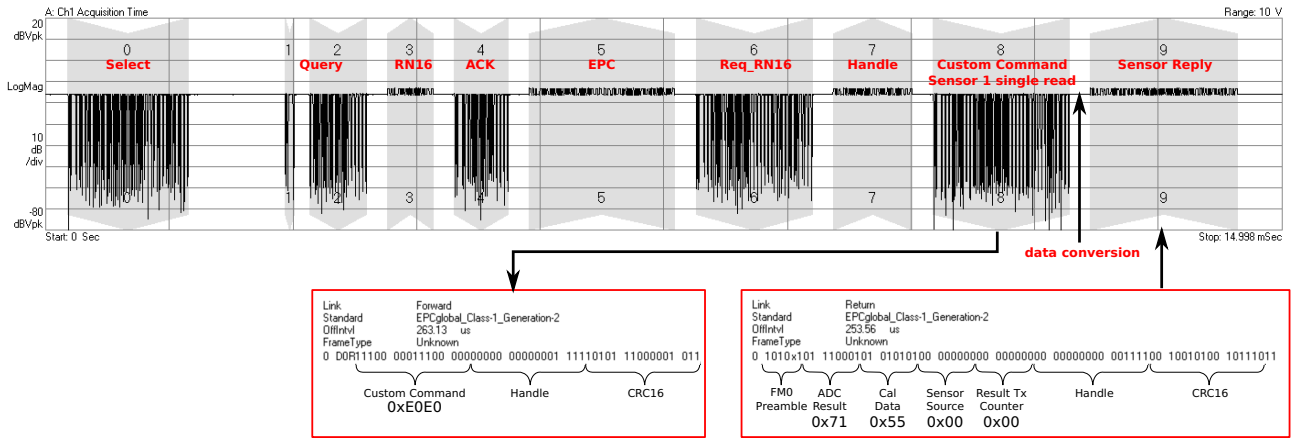


Fig. 17. Trace of a complete EPC-compliant communication with sensor custom command. A single sensor value is requested.

consumes as less energy as measured in the stand-alone setup. Fig. 17 depicts a trace of a sensor challenge and reply recorded with the Agilent VSA Software using the RFID demod option. The sequence up to the *Handle* is absolutely compliant to an inventory round of the EPC protocol. In data block 7 the custom command is sent requesting a single data conversion of sensor source '0'. The reply is sent directly after conversion (data block 8) containing an ADC result of 0x71, calibration data (0x55) and the sensor source information (0x00).

VIII. Conclusions

In this paper a novel multistandard RFID-tag has been presented. The tag features a HF/ UHF analog frontend including an UHF rectifier with a peak efficiency of 43%. Furthermore a sensor interface is integrated on the RFID-tag. The interface consists of temperature sensor, a multiplexer and an analog-to-digital converter. For ultra-low power operation a time-domain comparator has been used in the SAR ADC design. The overall static performance of the ADC is a DNL between -0.36 and +0.81 LSB. The corresponding INL lies between -0.75 and +0.75 LSB at a typical power consumption of less than 700 nW. Furthermore a distance measurement by means of modulated reflection is included in the tag. The incoming FMCW signal is modulated with a 300 kHz signal, which enables the differentiation between the wanted reflection of the tag and the unwanted reflection of the radar signal at other obstacles.

Acknowledgement

The circuit was developed jointly at the Institute for Electronics Engineering and the Infineon Design Center Graz (Austria) within the scope of a research project supported by the Bavarian Research Foundation. The FMCW reader was developed by Siemens CT in Munich.

References

[1] R. Martinez-Catala and J. Barrett, "A modular wireless sensor platform with fully integrated battery," *IEEE Transactions on Components and Packaging Technologies*, vol. 32, no. 3, pp. 617–626, 2009.

[2] U. Karthaus and M. Fischer, "Fully integrated passive uhf rfid transponder ic with 16.7- uw minimum rf input power," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1602–1608, oct. 2003.

[3] K. Seemann and R. Weigel, "The system design of integrated passive transponder devices," in *Asia-Pacific Microwave Conference*. IEEE, 2006, pp. 1114–1117.

[4] EPCglobal, "Radio-frequency identity protocols - class-1 generation-2 rfid v1.2.0," EPCglobal Standard, EPCglobal Inc., Mar. 2007. [Online]. Available: http://www.epcglobalinc.org/standards/uhfc1g2

[5] D. Pardo, A. Vaz, S. Gil, J. Gomez, A. Ubarretxena, D. Puente, R. Morales-Ramos, A. Garcia-Alonso, and R. Berenguer, "Design criteria for full passive long range UHF RFID sensor for human body temperature monitoring," in *RFID, 2007. IEEE International Conference on*, Mar. 26–28, 2007, pp. 141–148.

[6] J. Heidrich, D. Brenk, J. Essel, G. Hofer, G. Holweg, G. Fischer, and R. Weigel, "Low voltage reference cells for uhf transponders with advanced features," in *Proc. IEEE International Conference on Microwaves, Communications, Antennas and Electronics Systems COMCAS 2009*, 9–11 Nov. 2009, pp. 1–8.

[7] I. Filanovsky and S. T. Lim, "Interaction of threshold voltage and mobility temperature dependencies applied to stabilization of current and voltage," in *Proc. 43rd IEEE Midwest Symposium on Circuits and Systems*, vol. 3, 8–11 Aug. 2000, pp. 1022–1025.

[8] D. Brenk, J. Essel, J. Heidrich, and R. Weigel, "Ultra low-power techniques for sensor-enhanced rfid tags," in *IEEE MTT-S International Microwave Workshop on Wireless Sensing, Local Positioning, and RFID (IMWS2009)*, Sep. 2009.

[9] A. Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti, "A 9.4-enob 1v 3.8uw 100ks/s sar adc with time-domain comparator," in *Proc. Digest of Technical Papers. IEEE International Solid-State Circuits Conference ISSCC 2008*, 2008, pp. 246–610.

[10] J. McCreary and P. Gray, "All-mos charge redistribution analog-to-digital conversion techniques. i," *IEEE Journal of Solid-State Circuits*, vol. 10, no. 6, pp. 371–379, 1975.

[11] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd ed. Oxford University Press, 2002.

[12] F. Maloberti, *Data Converters*. Springer, 2007.

[13] I. Filanovsky and S. T. Lim, "Temperature sensor applications of diode-connected mos transistors," in *Proc. IEEE International Symposium on Circuits and Systems ISCAS 2002*, vol. 2, 26–29 May 2002, pp. II–149–II–152.

[14] Y. Zhai, S. Prakash, M. Cohen, and P. Abshire, "Detection of on-chip temperature gradient using a 1.5v low power cmos temperature sensor," in *Proc. IEEE International Symposium on Circuits and Systems ISCAS 2006*, 2006, pp. 4 pp.–.

[15] D. K. Barton, *Radar Systems Analysis and Modeling*. Boston, London: Artech House, 2005.

[16] L. Wiebking, *Entwicklung eines zentimetergenauen mehrdimensionalen Nahbereichs-Navigationssystems*. Duesseldorf: VDI Verlag GmbH, 2003.